SIGE HETEROJUNCTION BIPOLAR TRANSISTOR MULTI-FINGER STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to a semiconductor device structure and the manufacturing process thereof, more particularly to the design and fabrication of a high driving current multi finger bipolar transistor device.

2. Description of Related Art

In radio frequency (RF) application, higher device cut off frequency (f_T) is needed. Although higher f_T can be achieved by advanced RFCMOS technology, it is still unable to fully satisfy RF application requirement. For example, it is difficult to get f_T above 40 GHz. It is also very costly to develop advanced CMOS technology to get higher f_T. The devices with compound semiconductor material can get very high f_T, but the usage is restricted due to higher material cost, lower wafer size and poisonous nature of most of compound semiconductor material.

SiGe HBT is a good choice of high f_T devices. Firstly, the emitter injection efficiency and current gain can be increased due to band gap difference of SiGe base to silicon emitter. Secondly, base resistance can be reduced and f_T can be increased by heavily doped SiGe base. Lastly, SiGe module is compatible with silicon process. Now SiGe HBT is widely used in high f_T device application.

As illustrated in FIG. **1**, a multi-finger structure is used in existing SiGe HBT to increase current driving capability. To realize such a multi-finger structure, arrange the emitter (E) or the base (B) at the center, and symmetrically arrange bases or emitters at both sides of the central emitter or base, in a formation as C/BE/BE...BE/B/C, wherein, a base (B) is used by neighboring emitters, collectors (C) are formed at both ends of the structure, and the two collectors are connected to each other by a deep buried layer formed below the multi-finger structure, so that an overall multi-finger device structure is finally finished.

FIG. **2** illustrates a single device structure of an existing SiGe HBT multi-finger device, which includes collector **114**, base **111**, and emitter **110**. The collector **114** is a medium doped or low doped n type epitaxial layer formed on top of the n type heavily doped buried layer **102**. The collector **114** is connected to a metal electrode **107** through the n type heavily doped buried layer **102**, the n type heavily doped collector pick up **104**, and the contact **106**, wherein, the n type heavily doped buried layer **102** is formed on top of the substrate **101**; the n type heavily doped collector pick up **104** is in the active region; the contact **106** is formed through the interlayer dielectric **105**. The n type heavily doped collector pick up **104** is formed by a high dose and high energy ion implantation. The area of the collector pick up **104** is large, so that the sidewall capacitance of the collector is also large. Both sides of the collector **114** are isolated by shallow trench oxide **103**. Due to the large area of the buried layer, a deep trench **115** filled with polysilicon is added to the bottom of the shallow trench oxide **103** between devices to reduce the collector to substrate parasitic capacitance. The base **111** is a p type in situ doped SiGe epitaxial layer; the base **111** is connected to the electrode through a polysilicon layer **108** and a contact. A silicon oxide dielectric layer **113** is formed below the polysilicon layer **108**. The emitter **110** is consisted of an n type heavily doped polysilicon layer formed on top of the base **111**. Silicon oxide spacers **112** are formed at both sidewalls of the emitter **111**. The contact area between the emitter **110** and the base **111** is determined by the window size of the silicon oxide dielectric layer **109**. When opening the emitter window, selective ion implantation at the center of the collector which just enclose the emitter window can be performed to adjust breakdown voltage and cut off frequency of the SiGe HBT. To keep cut off frequency less affected, when multi-finger structure is adopted to increase the current driving capability, collectors should be arranged at the outmost sides of the whole device structure, as shown in FIG. **1**.

This SiGe HBT multi-finger structure is reliable and widely used. But the main disadvantages are: a buried layer of large size is formed through the whole multi-finger device to connect the two collectors at the outmost sides, which leads to large junction capacitance, and impacts the device speed. In the meantime, due to a great number of emitters but only few collectors, the current is concentrated in the buried layer and in the collector electrode, the collector junction size needs to be increased to avoid too high current density, which further increases the junction capacitance. Thus a multi-finger device structure only adopts two collector electrodes at both ends instead of multiple collectors in order not to increase junction area and impact device speed.

SUMMARY OF THE INVENTION

The objective of the present invention is to provide a SiGe HBT multi-finger structure, which can reduce capacitance, decrease collector output resistance, and improve frequency characteristics.

To achieve the aforementioned objective, the SiGe HBT multi-finger structure of the present invention is consisted of a plurality of SiGe HBT single cells; the multi-finger structure can be expressed as C/BEBC/BEBC/.../C, wherein C, B and E respectively represents a collector, a base and an emitter of a SiGe HBT, and CBEBC represents a SiGe HBT single cell; two neighboring SiGe HBT single cells share a same collector. The active region of a SiGe HBT single cell is isolated by field oxide shallow trenches, wherein a SiGe HBT single cell comprises: a collector region, consisting of an n type ion impurity implanted layer formed in the active region, the bottom of the collector region being connected to a buried layer formed by two n type pseudo buried layers at both sides of the active region, the collector region being connected to two collectors through the two n type pseudo buried layers and two deep trench contacts formed in the field oxide above the n type pseudo buried layers; a base region, consisting of a p type SiGe epitaxial layer formed on top of the collector region, the base region being connected to two bases through two polysilicon layers at both sides of the base region and two metal contacts formed on the polysilicon layers; and an emitter region, consisting of an n type polysilicon layer formed on top of the base region, the emitter region being connected to an emitter through a metal contact formed on top of the emitter region.

The n type pseudo buried layers are formed by n type ion impurity implantation, wherein the n type ion impurity is phosphorus. The dosage of the n type ion impurity implantation is 1e14~1e16 cm^{-2}, and the energy is 2~50 KeV. During the implantation of the pseudo buried layers, the top of the active region is protected by a hard mask, and the sidewalls of the active region are protected by sidewall spacers to prevent ion impurity from implanting into the active region. The hard mask is consisted of three dielectric layers, which are from the bottom up a silicon oxide layer, a silicon nitride layer, and a silicon oxide layer. The thicknesses of the three dielectric layers from the bottom up are respectively in the ranges of 100 Å~300 Å, 200 Å~500 Å, and 300 Å~800 Å; the thicknesses are determined by the energy of the n type ion impurity